Amendments to the Claim

Please amend claims 44 and add claims 51-56 as shown in the claim set below. Please cancel claims 24-30 and 43.

1-23. (Non-elected)

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24-30. (Cancelled)

31. (Original) An integrated circuit, comprising:

a programmable logic array (PLA) depopulated to include programmable connections only where required to implement certain known functionality and selectively minimally repopulated to accommodate future programming of other functionality.

32. (Original) The integrated circuit of claim 31, wherein:

the PLA programmed with the known functionality has certain performance characteristics, and wherein the PLA programmed with other functionality has the same performance characteristics.

33. (Original) The integrated circuit of claim 31, wherein:

the programmable connections include a storage device and a logic gate;

the PLA includes product terms and sum terms formed with gate trees.

34. (Original) The integrated circuit of claim 33, wherein:

the storage device is one of a latch or a flip-flop; and

the logic gate is an OR gate.

35. (Original) The integrated circuit of claim 33, wherein:

the storage device is one of a latch or a flip-flop; and

the logic gate is a multiplexer.

A1 cont.

36. (Original) The integrated circuit of claim 31, wherein:

the programmable connections include a pair of storage devices and a multiplexer.

37. (Original) The integrated circuit of claim 31, wherein the PLA includes:

an AND array with a first type of programmable connection; and

an OR array with a second type of programmable connection.

38. (Original) The integrated circuit of claim 31, wherein the PLA includes:

an AND array with programmable connections that each include a pair of storage devices and a multiplexer; and

an OR array with programmable connections that each include only one storage device and a logic gate.

39. (Original) The integrated circuit of claim 31, wherein the PLA includes: programmable connections for shared terms, spare terms, and complemented terms.

40. (Original) An integrated circuit, comprising:

a programmable logic array (PLA) having a depopulated array that includes programmable connections only where required to implement certain known functionality and selectively minimally repopulated to accommodate future programming of other functionality.

41. (Original) The integrated circuit of claim 40, wherein the depopulated array is an AND array.

A1 cont.

42. (Original) The integrated circuit of claim 40, wherein the depopulated array is an OR array

43. (Cancelled)

44. (Currently Amended) ~~The programmable logic array of claim 43,~~ A programmable logic array of including:

programmable connections that include a storage device and a logic gate; and

product terms that include a gate tree; wherein:

the storage device is one of a latch or a flip-flop;

the logic gate is one of a multiplexer or an OR gate.

45. (Original) A programmable logic array, including:

programmable connections that include a pair of storage devices and a multiplexer.

46. (Original) The programmable logic array of claim 45, further including:

product terms formed with AND trees; and

sum terms formed with OR trees.

47. (Original) A programmable logic array (PLA), including:

an AND array that includes a first type of programmable connection; and

an OR array that includes a second type of programmable connection.

48. (Original) The PLA of claim 47, wherein:

the first type of programmable connection includes a pair of storage devices and a multiplexer;

A1 cont.

the second type of programmable connection includes only one storage device and a logic gate.

49-50. (Non-elected)

51. (New) An integrated circuit, comprising:

a programmable logic array (PLA) having a depopulated array that includes programmable connections only where required to implement certain known functionality.

52. (New) The integrated circuit of claim 51, wherein the depopulated array is an AND array.

53. (New) The integrated circuit of claim 51, wherein the depopulated array is an OR array.

54. (New) The integrated circuit of claim 51, wherein the PLA includes:

programmable connections that include a storage device and a logic gate; and

product terms and sum terms formed with gate trees.

55. (New) The integrated circuit of claim 51, wherein the PLA includes programmable connections that include:

A1

a pair of storage devices; and

a multiplexer.

56. (New) The integrated circuit of claim 51, wherein the PLA includes:

an AND array that includes programmable connections that each include a pair of storage devices and a multiplexer; and

an OR array that includes programmable connections that each include only one storage device and a logic gate.